Eric R. Keller

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RESEARCH INTEREST

I design and build secure and reliable networked systems using a cross-layer approach that draws from networking, operating systems, distributed systems, and computer architecture. My focus is on virtualization and the movement toward cloud-based services.

EDUCATION

Ph. D., Princeton University, Electrical Engineering, 2011

Award:	Intel PhD Fellowship (2010-2011)
Advisor:	Jennifer Rexford
Dissertation:	Refactoring Router Software to Minimize Disruption

M.S., University of Massachusetts-Amherst, Electrical and Computer Engineering, 2005

Advisor:	Russell Tessier
Thesis:	Programming Model for Network Processing on an FPGA

B.S., Virginia Tech, Computer Engineering, 1999

RESEARCH EXPERIENCE

For more details, see http://www.changetheassumptions.com/projects.php

University of Pennsylvania, Post-doctoral researcher (2011-present)

- Advisor: Jonathan Smith
- Researching dependable networked services through the examination of both the security threats of virtualized environments (e.g., the threat of insider attacks in cloud infrastructures), and the opportunities for applying virtualization technology (e.g., applying virtualization to new domains such as cognitive radio).
- Applied for an NSF Medium grant, in the process of applying for another NSF grant, and involved in a large project awarded a grant under the DARPA Mission-oriented Resilient Cloud program.

Princeton University, Graduate researcher (2006-2011)

- Advisor: Jennifer Rexford
- Researched the application of virtualization to the core Internet and the security of virtualization technology.

Xilinx, Inc, (1999-2006)

- Researched run-time reconfiguration, system level design, and tools for networking specific applications.

TEACHING EXPERIENCE

- Teaching assistant for Princeton COS 109, “Computers in our world”
- Currently helping to advise five graduate students and previously helped advise 3 undergraduate students.
- Guest lecturer in Princeton COS 561 “Advanced computer networks”

PUBLICATIONS

2011 **Eliminating the Hypervisor Attack Surface for a More Secure Cloud**
Jakub Szefer, Eric Keller, Jennifer Rexford, and Ruby B. Lee
In Proc. ACM Conference on Computer and Communications Security (CCS). Oct., 2011.

2010 **NoHype: Virtualized cloud infrastructure without the virtualization**
Eric Keller, Jakub Szefer, Jennifer Rexford, and Ruby B. Lee
In Proc. International Symposium on Computer Architecture (ISCA). July, 2010.

Seamless BGP Migration with Router Grafting
Eric Keller, Jennifer Rexford, and Jacobus van der Merwe
In Proc. Networked Systems Design and Implementation (NSDI). Apr., 2010.

The 'Platform as a Service' model for networking
Eric Keller and Jennifer Rexford
In Proc. INM/WREN workshop. Apr., 2010.

2009 **Virtually Eliminating Router Bugs**
Eric Keller, Minlan Yu, Matthew Caesar, and Jennifer Rexford
In Proc. Conference on emerging Networking EXperiments and Technologies (CoNEXT). Dec., 2009.

Better by a HAIR: Hardware-Amenable Internet Routing
Firat Kiyak, Brent Mochizuki, Eric Keller, and Matthew Caesar
In Proc. IEEE International Conference on Network Protocols (ICNP). Oct., 2009.

Accountability in hosted virtual networks
Eric Keller, Ruby Lee, and Jennifer Rexford
In Proc. Workshop on Virtualized Infrastructure Systems and Architectures (VISA). Aug., 2009.

2008 **Virtual Routers on the Move: Live Router Migration as a Network-Management Primitive**
Yi Wang, Eric Keller, Brian Biskeborn, Jacobus van der Merwe, Jennifer Rexford
In Proc. ACM SIGCOMM. Aug., 2008.

Virtualizing the Data Plane Through Source Code Merging
Eric Keller and Evan Green
In Proc. PRESTO workshop. Aug., 2008.

2004 **Programming a Hyper-Programmable Architectures for Networked Systems**
Eric Keller and Gordon Brebner
In Proc. International Conference on Field-Programmable Technology (FPT). Dec., 2004.

Hyper-Programmable Architectures for Adaptable Networked Systems
Gordon Brebner, Phil James-Roxby, Eric Keller, Chidamber Kulkarni
In Proc. IEEE Conf. on Application-specific Systems, Architectures and Processors (ASAP). Sept., 2004.

2003 **Software Decelerators**
Eric Keller, Gordon Brebner, Phil James-Roxby
In Proc. 13th International Field Programmable Logic and Applications Conference (FPL). Sept., 2003.

A Self-Reconfiguring Platform
Brandon Blodget, Philip James-Roxby, Eric Keller, Scott McMillan, Prasanna Sundararajaran
In Proc. 13th International Field Programmable Logic and Applications Conference (FPL). Sept., 2003.

2002 **Gene Matching Using JBits**
Steven A. Guccione and Eric Keller
In Proc. 12th International Field-Programmable Logic and Applications Conference (FPL). Sept., 2002.

An FPGA Wire Data-Base for Run-Time Routers
Eric Keller and Scott McMillan
In Proc. Military and Aerospace Applications of Programmable Logic Devices (MAPLD). Sept., 2002.

2001 **Building Asynchronous Circuits With JBits**
Eric Keller
In Proc. 11th International Field-Programmable Logic and Applications Conference (FPL). Aug., 2001.

Run-Time Reconfigurable 2D Discrete Wavelet Transform Using JBits
Jonathan Ballagh, Peter Athanas, and Eric Keller
In Proc. Reconfigurable Technology: FPGAs for Computing and Applications II. Aug., 2001.

Java Debug Hardware Models using JBits
Jonathan Ballagh, Peter Athanas, and Eric Keller
In Proc. 8th Reconfigurable Architectures Workshop (RAW 2001). May, 2001.

2000 **Dynamic Circuit Specialization of a CORDIC Processor**
Eric Keller
In Proc. Reconfigurable Technology: FPGAs for Computing and Applications II. Nov., 2000.

JRoute: A Run-Time Routing API for FPGA Hardware
Eric Keller
In Proc. 7th Reconfigurable Architectures Workshop (RAW 2000). May, 2000.

INVITED TALKS

NoHype: Virtualized Cloud Infrastructure without the Virtualization
- University of Pennsylvania, Apr. 2011.
- IBM, Dec. 2010.

Dynamic Infrastructure for Dependable Cloud Services
- University of Maryland, Mar. 2011.
- Northeastern University, Mar. 2011.
- Bell Labs, Feb. 2011.
- University of Delaware, Feb. 2011.
- Rutgers University, Dec. 2010.

Refactoring Router Software to Minimize Disruption
(Earlier title: Migrating and Grafting Routers to Accommodate Change)
- Georgetown University, Nov. 2011.
- University of North Carolina, Mar. 2010.
- Rutgers University, Mar. 2010.
- University of Pennsylvania, Jan. 2010.
- North Carolina State University, Dec. 2010.
- Duke University, Nov. 2010.
- Bell Labs, Jan. 2010

Accountability in Hosted Virtual Networks
- Microsoft Research, Jul. 2009.
- AT&T Research, Jul. 2009.

SERVICE

- Member of Shadow Program Committee for International Conference on emerging Networking EXperiments and Technologies (CoNEXT) 2011.
- External reviewer for NSDI 2010, HPCA 2010, SIGCOMM 2009, USENIX ATC 2009, IEEE CCNC 2009.
- Program Committee Member for NetFPGA Developers Workshop 2009 and 2010.
- Scribe for NSDI 2009, PRESTO 2007.

PATENTS

- *8,032,874* – "Generation of executable threads having source code specifications that describe network packets"
- *7,990,867* – "Pipeline for processing network packets"
- *7,823,162* – "Thread circuits and a broadcast channel in programmable logic"
- *7,792,117* – "Method for simulating a processor of network packets"
- *7,788,402* – "Circuit for modification of a network packet by insertion or removal of a data segment"
- *7,784,014* – "Generation of a specification of a network packet processor"
- *7,770,179* – "Method and apparatus for multithreading on a programmable logic device"
- *7,698,449* – "Method and apparatus for configuring a processor embedded in an integrated circuit for use as a logic element"
- 7,689,726 – "Bootable integrated circuit device for readback encoding of configuration data"
- *7,653,895* – "Memory arrangement for message processing by a plurality of threads"
- *7,574,680* – "Method and apparatus for application-specific programmable memory architecture and interconnection network on a chip"
- *7,552,042* – "Method for message processing on a programmable logic device"
- *7,386,826* – "Using redundant routing to reduce susceptibility to single event upsets in PLD designs"
- *7,328,335* – "Bootable programmable logic device for internal decoding of encoded configuration data"
- *7,228,520* – "Method and apparatus for a programmable interface of a soft platform on a programmable logic device"
- *7,227,378* – "Reconfiguration of a programmable logic device using internal control"
- *7,185,309* – "Method and apparatus for application-specific programmable memory architecture and interconnection network on a chip"
- *7,131,077* – "Using an embedded processor to implement a finite state machine"
- *7,111,215* – "Methods of reducing the susceptibility of PLD designs to single event upsets"
- *7,076,596* – "Method of and apparatus for enabling a hardware module to interact with a data structure"
- *7,028,283* – "Method of using a hardware library in a programmable logic device"
- *7,010,664* – "Configurable address generator and circuit using same"
- *6,920,627* – "Reconfiguration of a programmable logic device using internal control"
- *6,883,147* – "Method and system for generating a circuit design including a peripheral component connected to a bus"
- *6,725,441* – "Method and apparatus for defining and modifying connections between logic cores implemented on programmable logic devices"
- *6,487,709* – "Run-Time Routing for Programmable Logic Devices"

REFERENCES

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Prof. Ruby B. Lee
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